Analysis of ESD Protection Technology of Integrated Circuits

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Abstract: With the continuous advancement of technology, economy and other aspects, the scope of application of integrated circuits has been expanded, the technology of chip technology has been improved, and the performance advantages of chips have been fully demonstrated. On the other hand, static and discharge phenomena have occurred since the application of new process chips, which has reduced the ESD tolerance, and ESD protection should be increased. Rationally plan ESD protection circuits to promote the development of ESD.

1. Introduction

In the process of using special processes, a variety of circuit components are incorporated and they are spliced together, such as resistors, transistors, capacitors and inductors, to evolve into a micro-structure and have corresponding circuit functions. With the innovation and development of integrated circuits, although the current electronic components are gradually becoming more and more miniaturized, intelligent and reliable, the problem that needs to be dealt with is still the ESD phenomenon. In this regard, this paper discusses the integrated circuit ESD protection technology in detail, and explores the relevant means to extend the life of the integrated circuit and manufacturing.

2. ESD protection technology necessity

According to the data, the relevant economic losses generated by the release of static electricity in China every year have risen to one billion US dollars. Due to the excessive cost of the loss, ESD protection technology was used in the production of the product, and the effect was remarkable. Through the analysis and research of the manufacturing and electronics industries, the need for ESD protection technology has been summarized. (1) The use of ESD protection technology in the manufacturing industry can remove dust to a certain extent, protect components from damage, reduce the casualty rate, prevent fire and explosion events, avoid product loss, and operate safely and smoothly. (2) The use of ESD protection technology in the electronics industry can not only enhance the quality of electronic products, extend the life of circuits, protect the safety of workers, but also improve the overall economic efficiency of enterprises, and increase the risk management of enterprises.

3. Design principles in ESD protection circuits

When the circuit is in normal operation, it must be ensured that the part is closed, so that the ESD problem will not be induced. The reason is that there is a certain relationship between the circuit and the ESD device contact voltage. Once triggered, serious core circuit problems will occur. Especially when the ESD problem occurs in the microelectronic chip, it is necessary to increase the protection of the device, and use the second level expansion calculation, for example, the ESD event induced frequency, such as the device charging model. When the protection circuit is in the off state, it is easy to damage the core circuit, and the design work of the ESD protection level is considered, so that the circuit is not damaged and is in good condition. When an ESD problem occurs, the protection device should be quickly turned off. If the shutdown is not timely, the device will be a latch-up condition that will maximize the display of the core circuit.

4. The cause of the ESD phenomenon of integrated circuits

There are many factors that cause the electrostatic discharge problem of integrated circuits, and the situation is very simple. If the electrostatic field is in contact with several different electrostatic potential objects, then the static charge will induce mutual transmission. At this time, the voltage formed by the electrostatic discharge. At around 3 kV, the energy it has is very high. In general, semiconductor devices and other components are common devices in integrated circuits, and they are extremely susceptible to damage due to voltage. Explain in detail the cause of the ESD phenomenon of the integrated circuit.

The electron attraction involved in the operation of the integrated circuit is obviously different. When two objects start to touch or are in a separated state, a triboelectric charge occurs. At this time, the charging charge contains electricity, and if the neutralization frequency is too slow or When too fast, a large amount of charge will be delivered, increasing the internal voltage height of the integrated circuit. The friction frequency, contact range, ambient air humidity and temperature of the charged object in this link will affect the triboelectric charge, thus reducing the ESD discharge amount.

In addition to the above-mentioned factors, in the external electrostatic field to place an unpowered integrated circuit, the location of the stolen electricity in the integrated circuit will be affected by the external electrostatic field, resulting in multiple separation of the moving charge. Based on this, when an unpowered integrated circuit and other conductive objects that are different from their own voltages are touched, the integrated circuit is thus affected by a short or excessive current, and then is in a state of charge. The current pulses formed at this time will be affected by time, amplitude environment, integrated circuits, and voltage.

5. Protective parts for integrated circuit ESD

5.1. Resistors

When the integrated circuit is in production and manufacturing, the resistors used are similar to those of passive devices, so there is no ESD problem with integrated circuits. In most cases, the N-type well resistor is used by the designer because the current in the N-well resistor is the same as the total current during the application phase. If the amount of electric field current is weak during the application process, there will be a certain linear relationship between the electric field strength and the current. If the electric field current is too strong, the current will be saturated.

5.2. Diode

The most common type of integrated circuit is a diode with a relatively high voltage clamping component. The structural frame of the component is extremely advantageous. Diodes can be added when ESD problems occur in the circuit. Because the diodes do not have hysteresis characteristics, rail-to-rail protection is chosen. This type of protection network highlights its own rigor and achieves the desired results. Further research and discussion of the diode application steps, found that the current in the tube when the diode is used in the integrated circuit is only 0.7 volts, which can better solve the problem of ESD current discharge. However, when standing in oppositional analysis, the diode breakdown voltage is high, and the reverse diode protection ability is weakened. In order to improve the protection effect of the integrated circuit, the diode forward direction is used in the process of applying the diode.

5.3. Bipolar transistor

Bipolar transistors are part of a guard period with a forward biased pn junction and a reverse biased pn junction. Bipolar transistors forward bias the pn junction during operation to increase the current carrying around the reverse biased pn junction. child. Because the reverse biased pn junction current is affected by a small number of carriers, based on the forward biased pn junction field of view, a relatively large number of carriers are collected, raising the concentration around the carrier. At this time, the current in the bipolar transistor will gradually increase, so it is important to protect

the components in the integrated circuit.

6. Common problems in ESD protection technology

Staff professional quality and safety awareness is poor. At this stage, the electrostatic protection technology is frequently applied in many enterprises, and the technology is paid more and more attention. However, due to the poor professional quality and safety awareness of the staff, the work efficiency has not been improved. On the one hand, enterprises do not pay enough attention to the training of electrostatic protection quality. Many employees lack the corresponding professional knowledge. When they encounter an emergency, they cannot calmly deal with it, so they adopt appropriate methods to deal with them. On the other hand, most of the employees in the electronics industry do not follow the static management standards in the process of producing electronic products. For example, metal objects such as necklaces and rings are worn many times during normal work.

The degree of automation of electrostatic protection is low. Along with the rapid development of artificial intelligence, Internet of Things and other modern information technology industries, although many enterprises have achieved the goal of electrostatic protection automation degree, there are still some small-scale electronic production enterprises in the initial stage of electrostatic protection measures, making the production quality of enterprise products rapidly down.

7. Relevant ESD protection technology using improved methods

Strengthen the professional quality and safety awareness of employees. Due to the poor professional quality and safety awareness of employees within the company, electronic companies need to choose various effective methods to strengthen their professional quality and safety awareness. On the one hand, enterprises need to organize electronic technicians to participate in training and education activities on time, and fundamentally improve the quality of electronic technicians. On the other hand, enterprises should inform employees of the dangers of static electricity, and carry out one-on-one training. When faced with the situation of static electricity, they should grasp the emergency treatment methods, so as to achieve the purpose of improving personnel safety awareness and avoid more deaths and injuries.

Improve the automation level of small electronic enterprises. With the passage of time, people's quality of life has been significantly improved, and the development of science and technology is advancing by leaps and bounds. The most common method used in electrostatic protection work is automated static monitoring. Automated static monitoring can reduce the funds of static protection personnel to a certain extent, reduce the damage rate of static electricity to products, and increase the qualified rate of products, thus promoting the development of enterprises. It can be seen that if small electronic enterprises want to strengthen the level of static protection, they should actively introduce and scientifically use automated monitoring equipment to quickly improve their automation level.

8. Analysis of ESD protection technology of integrated circuits

8.1. SCR protection technology

In the ESD protection of integrated circuits, thyristors are the most common zero devices. They are a kind of protective parts. The SCR components are placed in integrated circuits. Usually, relatively simplified thyristors are used. The main types of resistors are N-type wells and P-type wells, there are two injection areas on both sides, N-type well resistance P+ injection, N+ injection will be directly connected in the integrated circuit anode port, P-type well resistance P+ injection, N+ injection will be connected into the integrated circuit cathode port. After further research and discussion of the thyristor structure, it can be seen that the number of resistors and parasitic transistors included in the application of the protection technology is two. In the ESD protection phase of the integrated circuit, the thyristor can be used at the same time, which is regarded as the

two end parts and connected in the integrated circuit. Connect the cathode and P-well, anode and N-well.

Although thyristors and integrated circuits have been reinforced again, the ESD capability of the core circuits is relatively relieved in integrated circuits. Such problems do not help at all stages of the integrated circuit application, so in the process of applying SCR protection technology. To ensure that the thyristor is not damaged, and thus better protect the integrated circuit current and voltage. In order to be able to use SCR protection technology scientifically and reasonably in integrated circuits, it fully reflects its protection value. During the process of connecting the thyristor and the bipolar transistor Pn, it is bound to contact the thyristor to further enhance the protection effect.

8.2. Full chip protection technology

Further discussion and research on the ESD phenomenon, if this phenomenon is too serious, it will destroy the integrated circuit and cause irreversible phenomena. In most cases, in order to improve the ESD protection capability of the integrated circuit, the ESD protection circuit is installed around the input PAD. Although the protection capability is improved, the internal problem in the integrated circuit is still a top priority and needs to be highly valued. Should increase the intensity of full chip protection technology. In the process of applying full-chip protection technology, technicians need to join PowerClamp. This circuit protection design can be used in the middle of VSS rail and VDD rail. At this time, PowerClamp protection circuit can be divided into dynamic circuit and static circuit. The current characteristics based on the static PowerClamp protection circuit are relatively fixed, which is convenient for the safe and stable operation of the integrated circuit. At this time, a fixed trigger voltage is required. If the source voltage is higher than the trigger voltage, the static PowerClamp protection circuit will be unblocked by the integrated circuit. At this time, the static electricity will discharge some current, which will be further protected by the protection device diode. Triggering the SCR circuit, the PowerClamp protection circuit consists of a diode string and an SCR circuit, which are the two most common circuits.

Relative to the full-chip protection technology of the PowerClamp protection circuit, further research and discussion are needed to find the best protection means to improve the protection effect. Based on the detection of ESD signals, a dynamic PowerClamp protection circuit will be generated. How to correctly judge the true and false ESD signal in the dynamic PowerClamp protection circuit is the key issue of its research. Only by putting the ESD signal judgment work in place can the ESD protection function be further improved.

8.3. Technical protection analysis

Static electricity is the most common form of damage in integrated circuits and can be broadly classified into two types: thermal failure and electrical failure. Thermal failure means that when the ESD current enters the inside of the chip directly through the chip pin, if the current intensity is very large, a large amount of heat will be generated in the small space of the chip, resulting in a rapid increase in the temperature of the region and a high temperature phenomenon. The chip is burned out, usually because of the thermal effect, and the burnt-out position generally exhibits diffusion resistance, polysilicon resistance, and interconnect resistance. The location of the electrical failure is usually not the value of the protection circuit, and has a certain ESD electrical high voltage effect in the internal circuit of the chip. If the gate oxide of the MOS transistor is exceeded, the thickness of the gate oxide in the internal circuit MOS transistor will be thinner. If a very high voltage is released on the very thin gate, the electric field power will be further enhanced, and the gate will be broken if it occurs on the diode. The effect will break the PN junction. In order to further prevent the internal circuit of the chip from being damaged by the ESD current, the current can be fully wound into the circuit inside the chip before the current is discharged, and can be implemented from another low resistance channel when released, and can be used when using the low resistance channel. The large current is completely released, and there is also a small voltage drop. This kind of behavior can cause the circuit inside the chip to not release the thermal

effect and not induce the electrical failure. According to the above suggestion, when the chip is in the normal state, the low-resistance channel is disconnected, and will be turned on when there is ESD voltage flowing. This problem needs to be highly valued.

8.4. Layout design perfect analysis

On the one hand, when designing the ESD layout, it should be as symmetrical as possible, and there should be no deviation. If the types of the pins are the same, then the same type of ESD protection circuit can be applied, and the contact hole density can be reasonably set to make uniform arrangement. In the deployment phase, the number of parasitic resistances on the interconnect line should be reduced as much as possible, and the interdigital structure should be applied to the diode ESD protection parts while increasing the circumference. On the other hand, the interdigitated structure method can be used when deploying the GDPMOS device and the GGNMOS device, so that the length and width of the interdigital finger do not exceed the prescribed range. SCR devices can be used in the selection of ESD protection devices to properly control the N+ diffusion area distance to prevent unnecessary trouble during the use phase.

9. Conclusion

In summary, with the continuous advancement of technology, economy and other aspects, the scope of application of integrated circuits has been expanded, and the chip process technology has been improved, fully demonstrating the performance advantages of the chip. There are many influencing factors in the analysis of integrated circuit chip ESD, and there are many problems. Therefore, we should further analyse the ESD protection methods, enhance the application value and scale in military regions and industrial areas, enhance the chip yield, highlight its reliability, promote the development of China's industrial undertakings and military undertakings, and contribute its own strength.

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